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Spin–Orbit-Torque-Driven Two-Terminal Giant Magnetoresistance Memristive Devices for In-Memory Computing

Tianli Jin,*,⊥ Bo Zhang,⊥ Dihua Wu, Eng Kang Koh, Funan Tan, Calvin Xiu Xian Lee, Ze Chen, Gerard Joseph Lim, Kaiming Cai, Jiangwei Cao,* and Wen Siang Lew*

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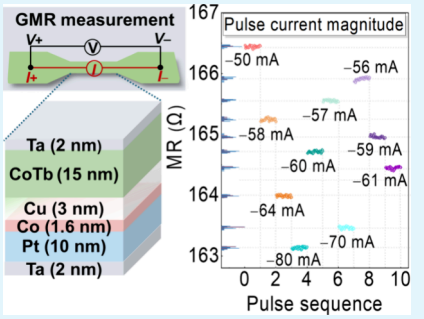
ABSTRACT: The rising complexity of artificial intelligence and data-intensive applications drives the demand for memristive devices to support high-performance and scalable processing-in-memory (PIM) architectures. While three- and four-terminal spintronic PIM solutions show promise, they face scalability challenges due to large footprints. This study demonstrates a two-terminal spin–orbit torque (SOT)-driven giant magnetoresistance (GMR) memristive device utilizing a Pt/Co/Cu/CoTb stack, integrating data storage and logic functions within a single unit. Ten nonvolatile resistance states are achieved by modulating the SOT current amplitude, and additional states with opposite polarities are created by tuning the CoTb alloy composition. Synaptic plasticity, including long-term potentiation and depression, is demonstrated through current pulse modulation. Simulations of a deep neural network constructed with this GMR device achieve 92% accuracy in handwritten digit recognition and image visualization tasks. Moreover, basic Boolean logic functions further showcase the processing capabilities. This two-terminal GMR device offers a scalable solution for advanced memristive memory and in-memory computing.



KEYWORDS: *GMR memristive device, multiple magnetization states, spin–orbit torque, artificial synapses, logic function*

1. INTRODUCTION

With the rise of big data-driven applications such as the Internet of Things (IoT) and artificial intelligence (AI), the challenge of achieving efficient information transmission and processing has become more pronounced.[1−3] Substantial efforts have been directed toward developing advanced AI chips using conventional technologies, such as developing Blackwell dynamic random-access memory and scaled-down transistors to increase chip power and efficiency.[4] However, this traditional von Neumann architecture separates memory and processing units, leading to low energy efficiency, as well as other issues related to quantum effects and reliability.[5−7] To address the physical separation between memory and processors, the concept of processing-in-memory (PIM) has garnered substantial interest from both the industry and academia.[8−10] The PIM architecture is a technology that embeds computing functions directly into memory. By seamlessly integrating compute units within the memory array, the PIM architecture can perform data processing operations internally within the memory. Memristors, possessing adjustable resistance characteristics, can store and process data by changing their resistance state. They are key components in building PIM architecture.[11−13] Various memristors have been proposed for PIM architecture, including phase change,[14] ferroelectric,[15] and resistive memristors.[16] Unlike these memristors, which store information relying on reversible phase transition, ferroelectric domain switching, the formation and rupture of conductive filaments and the modulation of oxygen vacancy concentration in transition metal oxides, spintronic memristors, utilizing spin degrees of freedom, show great potential as next-generation memristors owing to their low energy consumption, fast read/write speeds, nonvolatility, and high endurance.[17−22] Recent studies have explored the applications of spintronic memristors in Deep Neural Networks (DNNs), Spiking Neural Networks (SNNs), and Binary Neural Networks (BNNs), each leveraging the unique properties of spintronic devices tailored to their computational models.[23−25] In DNNs, which compute using continuous values, spintronic memristors are employed to store analogue synaptic weights. These weights can be dynamically updated based on the interaction between the connected preneurons and postneurons. The neurons in DNNs are typically activated using step functions, linear functions, or sigmoid transfer functions, enabling versatile computation.[26−28] In SNNs, which process information using spikes or discrete events instead of continuous activations, spintronic memristors serve as computational elements to

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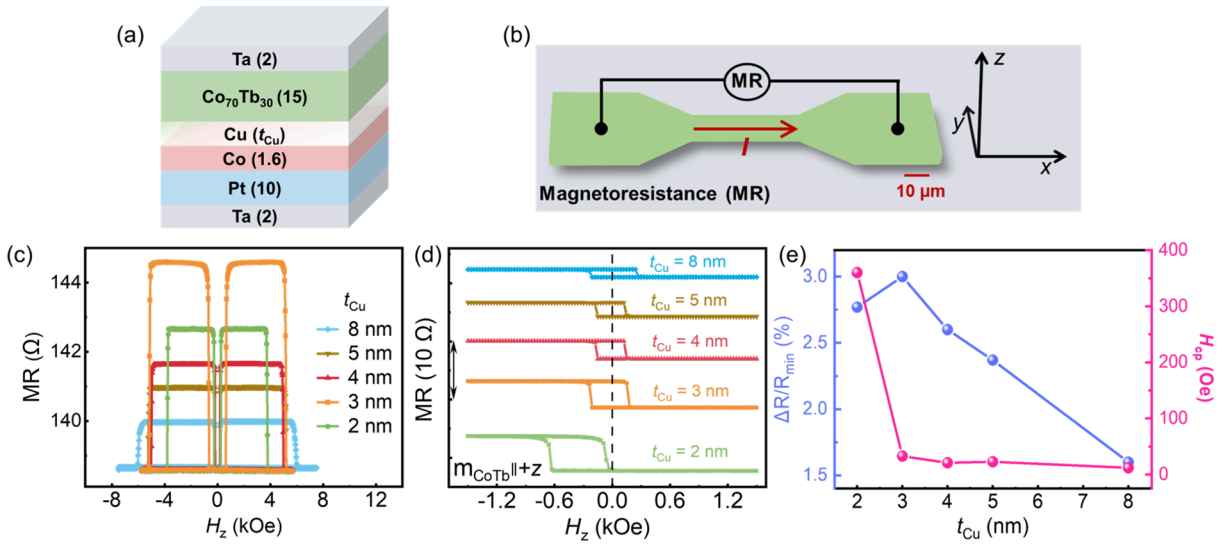

Figure 1. GMR memristive structure and output magnetoresistance (MR) signal with varying Cu thickness. (a) Schematic of the GMR memristive structure. (b) GMR memristive device configuration for MR measurement. (c) MR signals versus the perpendicular magnetic field for samples with different Cu thicknesses. (d) Estimation of the coupling strength between Co and CoTb layers within the minor loops, and the magnetization direction of the CoTb layer along + z direction. (e) Summary of the GMR ratio ($\Delta R/R_{min}$) and coupling strength (H_{cp}) as a function of the Cu thicknesses.

simulate spike-timing-dependent plasticity (STDP) synapses and neuron-like behavior. For BNNs, which operate on binary states instead of analog values, spintronic devices with bistable memory features are inefficient for PIM. To address this issue, stochastic binary synaptic devices, influenced by unavoidable thermal fluctuations, have been developed to enable probabilistic computation.[29,30] The switching probability of these devices under stimulation can be precisely tuned between 0 and 100% by adjusting the input signals. This probability-switching behavior mimics multiple states and enables the implementation of STDP properties.

To date, there are two primary approaches to improving the performance of spintronic memristors for DNNs and SNNs. One is to enhance spin−orbit torque (SOT) efficiency by reducing the operating current density.[31−34] The other is to increase the number of memristive states by modifying the magnetization reversal mode.[35−39] In these methods, information is typically read out in two ways. One way utilizes a four-terminal Hall cross structure, where Hall resistance serves as the indicator to monitor SOT-driven different magnetization states. However, changes in the ratio of Hall resistance are typically less than 1%, making it difficult to distinguish the actual signal from background noise and limiting detection sensitivity in signal readout. Additionally, using four-terminal Hall devices increases the footprint, resulting in scalability challenges and hindering their integration into miniaturized devices.[36−38] The other method utilizes tunnel magnetoresistance (TMR) structures, which provide a large readout signal.[40,41] For binary neural network applications, commercialized STT-MRAM with stochastic behavior demonstrates significant potential for practical use. However, achieving this stochastic behavior in TMR structures requires precise engineering of the free layer thickness and anisotropy energy to reduce the thermal stability factor below 15.[30,42] The fabrication process of 3-terminal TMR devices is inherently complex, involving precise control over tunnel barrier quality, multiple etching and deposition steps to achieve the separation of read and write paths in SOT-based MTJ.

In this study, a novel two-terminal GMR memristive device capable of achieving both memristive storage and logic functions within a single unit has been demonstrated. Featuring a perpendicularly magnetized Pt/Co/Cu/CoTb stack, the device utilizes SOT from the Pt layer for data writing and planar GMR for the readout. Such a proposed two-terminal GMR memristive device is efficient at performing analog synaptic weights for DNN, and the change of synaptic weights can be achieved by applying continuous positive (or negative) current pulses. The readout signal for this two-terminal memristive device is enhanced to 6.5% by optimizing the Cu interlayer and CoTb interface, demonstrating great potential for highly scalable in-memory computing. Moreover, ten resistance states for storage have been achieved by adjusting the SOT-driven current amplitude, and more memristor states with opposite polarity have been demonstrated by tuning the composition of the CoTb reference layer. Additionally, the STDP functionality of the synapse was achieved through current pulses, including long-term potentiation (LTP) and long-term depression (LTD). A fully connected DNN constructed using this GMR memristive device was simulated to achieve 92% accuracy in handwritten digit recognition, comparable to 95.5% accuracy from numerical analysis based on the ideal synapse. We also conduct the image visualization tests to utilize the discrete Fourier transform through this GMR device. Furthermore, successfully demonstrating basic Boolean logic operations within this two-terminal GMR memristive device further validates its computing functionality. These devices enable the development of all-electrical memory and logic systems, paving the way for advanced memristive memory applications through simplified fabrication processes and two-terminal device architecture.

2. RESULTS AND DISCUSSION

2.1. Enhancement of Readout Signals in the Co/Cu/CoTb Heterostructure. The GMR memristive structures with a full stack of Ta (2)/Pt (10)/Co (1.6)/Cu (t_{Cu})/

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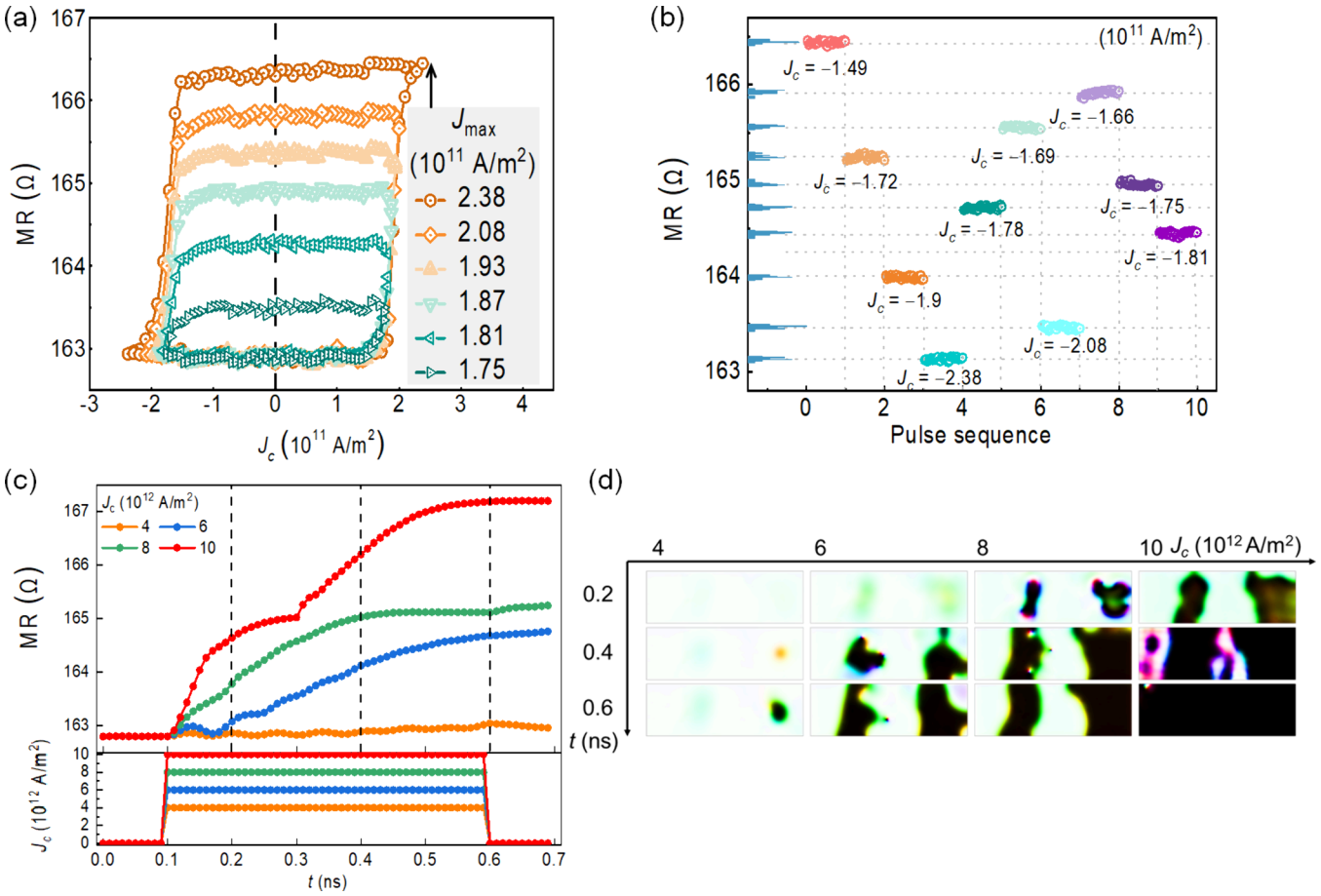

Figure 2. Demonstration of nonvolatile multiple memristive states in the Co (1.6 nm)/Cu (3 nm)/$Co_{70}Tb_{30}$ (15 nm) heterostructure. (a) Multiple MR states achieved by varying the amplitudes of the current pulse. (b) Demonstration of the distribution and stability of the ten states. (c) Simulated MR value under different current densities. (d) The snapshot of the magnetization state evolution of the Co layer over time under different current densities.

$Co_{70}Tb_{30}$ (15)/Ta (2) (units in nm) were deposited on the Si/SiO_2 substrate by using magnetron sputtering at room temperature, as illustrated in Figure 1a. The heavy metal Pt layer with a thickness of 10 nm serves as the SOT source layer. On top of the Pt layer, the 1.6 nm Co layer exhibits out-of-plane magnetic anisotropy due to its interfacial anisotropy, which acts as the free layer. The CoTb alloy with tunable magnetic moment polarity displays bulk perpendicular magnetic anisotropy, serving as the reference layer. The nonmagnetic Cu layer is used as the spacer layer for facilitating electron transport, tuning the output signal, and preventing direct magnetic interaction between Co and CoTb layers. The comparison of readout signals for different spacer layers in this GMR structure is provided in Supporting Information S1.

The GMR characterizations were carried out on two-terminal devices with dimensions of 10 μm × 100 μm, as presented in Figure 1b. The longitudinal magnetoresistance (MR) of these samples was measured by sweeping the magnetic field along the out-of-plane direction (H_z), and the test results are illustrated in Figure 1c. We observed a significant GMR signal, characterized by two resistance states depending on the relative magnetization orientation between the bottom Co and the top CoTb layers.[43,44] The magnitude of the GMR ratio varied with the thickness of the Cu layer. This ratio is defined as $\Delta R/R_{min}$, where ΔR represents the change in MR value from minimum to maximum, and R_{min} is the minimum value of MR. This relationship is summarized in Figure 1e. The $\Delta R/R_{min}$ first increases and then decreases with the Cu thickness, peaking at 3.01% when the Cu thickness is 3 nm. Consequently, we explored the coupling strength H_{cp} between the two magnetic layers by conducting minor loop tests within the H_z range of ±1.5 kOe. H_{cp} can be evaluated from the magnetic field shifting by fixing the magnetization direction of the CoTb layer along the $+z$ axis. These minor loops probed the relative changes in the magnetization state of the Co-free layer, as demonstrated in Figure 1d. When t_{Cu} = 2 and 3 nm, a distinct shift of the minor loops toward the $-H_z$ direction was observed. This shift indicates the presence of a positive external field H_z, resulting from the influence of the reference layer m_{CoTb} along the $+z$ direction, which can be attributed to the ferromagnetic coupling between the Co and CoTb layers. Figure 1e presents the relationship between H_{cp} and the thickness of the Cu layer. When t_{Cu} = 2 nm, the coupling between the two magnetic layers is strong and H_{cp} reaches up to 360 Oe. While for $t_{Cu} \geq 3$ nm, the H_{cp} is reduced to 12 Oe, indicating a weaker coupling between the two magnetic layers. Optimization of the ferromagnetic coupling via adjusting Cu thickness to 3 nm results in an enhancement of the readout signal to 3.01% in the Co/Cu/CoTb heterostructure.[43−45] Moreover, the use of interface engineering strategies to enhance the GMR ratio to 6.5% is discussed in Supporting Information S2.

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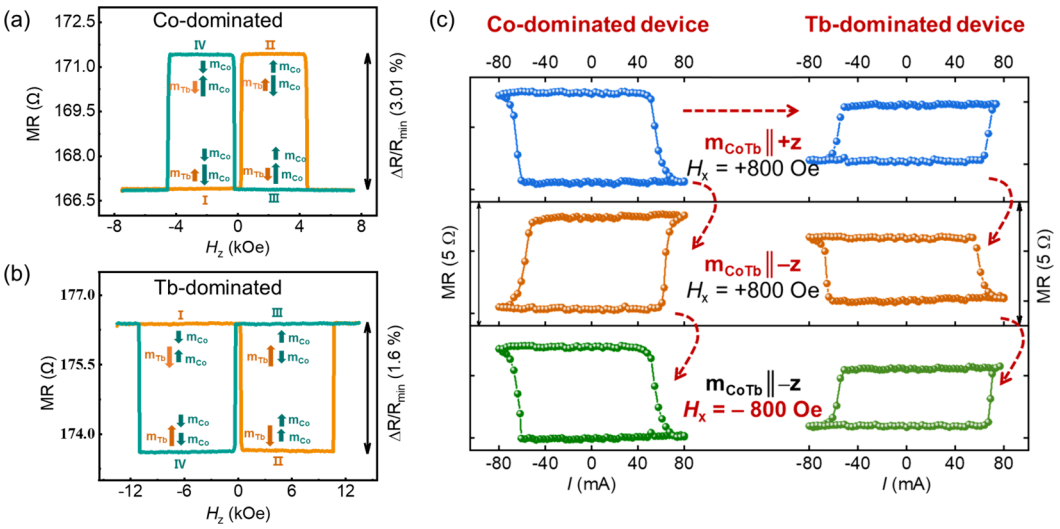

Figure 3. Demonstration of multiple memristive states by tuning the reference CoTb layer composition. (a) Magnetic field-induced MR change for the Co-dominated device. (b) Magnetic field-induced MR change for the Tb-dominated device. The green and yellow arrows indicate the magnetic moment of Co and Tb, respectively. (c) Current-induced magnetization switching behavior of the Co layer by controlling the initial magnetization orientation of the CoTb layer and H_x direction for Co-dominant and Tb-dominant devices.

2.2. Demonstration of Multiple Memristive States. With the high output signal observed in the Co (1.6 nm)/Cu (3 nm)/$Co_{70}Tb_{30}$ (15 nm) heterostructure, we investigate its potential for applications in multistate storage and DNN. To explore this capability, multistate storage tests were conducted on this device. Initially, an in-plane magnetic field of $H_x = -800$ Oe was applied, followed by a sequence of current pulses with varying maximum magnitude J_{max}, expanding from 1.75×10^{11} to 2.38×10^{11} A/m^2, were sent to this device. Corresponding to the J_{max} variations, distinct minor loops with varying MR values were observed, as shown in Figure 2a. This result demonstrates that different J_{max} settings can induce different intermediate magnetization states in the Co free layer, leading to changes in the relative magnetization orientations of Co and CoTb. The output MR value serves as an indicator, highlighting the versatility of the GMR memristive device in encoding multiple states within a single unit.

Next, we have implemented a nonvolatile 10-state by applying a pulse current to the GMR memristive device. Initially, the device was magnetized using a current density of $J_{SET} = +2.38 \times 10^{11}$ A/m^2 under $H_x = -800$ Oe. Subsequently, current pulses J_c with various amplitudes from -1.49×10^{11} to -2.38×10^{11} A/m^2 were applied to the device, and the output resistance was recorded 30 times after each pulse using a 3×10^{10} A/m^2 test current, as demonstrated in Figure 2b. Here, the ten current pulses have been simplified to a sequence from 1 to 10, and the amplitude of each pulse current has been labeled in the inset. The distribution of the ten states is displayed on the left side of Figure 2b. The results show that the two-terminal GMR device successfully achieved ten storage states, each exhibiting high stability. The multistate behavior of the GMR memristive device arises from the controlled positioning of domain walls within the Co-free layer, as verified by micromagnetic simulations. The SOT-driven torque originates from the heavy metal Pt layer via its spin Hall effect. When a pulsed charge current is applied, the resulting spin current exerts an antidamping torque on the adjacent Co layer, initiating domain wall nucleation and subsequently driving its motion. The output MR values are calculated using the equation, $MR = (R_P - R_{AP}) \times M_z/2 + (R_P + R_{AP})/2$, where M_z denotes the normalized magnetization along the z-direction, and R_P and R_{AP} denote the parallel and antiparallel resistances between the Co and CoTb layers, corresponding to the minimum and maximum MR values, respectively. Figure 2c presents the normalized magnetization change and the MR values under varying J_c, ranging from 4×10^{12} to 10×10^{12} A/m^2. Figure 2d displays the distinct magnetization configurations corresponding to the various applied current densities, confirming that the multistate GMR response is governed by the magnetization of the Co free layer. More details of micromagnetic simulations have been discussed in Supporting Information S3.

To gain insight into the effect of the CoTb layer on multiple memristive states, an investigation was conducted by modifying the composition of the CoTb reference alloy layer. Two typical samples, $Co_{70}Tb_{30}$ (Co-dominant) and $Co_{54}Tb_{46}$ (Tb-dominant), were prepared through cosputtering Co and Tb targets by varying the power supplied to the Co target. Figure3a,b shows that the MR signals change with H_z for $Co_{70}Tb_{30}$ and $Co_{54}Tb_{46}$ samples, respectively. The results of four distinct nonvolatile states are shown in both samples, with the orientation of magnetic moments corresponding to these states illustrated in the inset of Figure 3a,b. For the $Co_{70}Tb_{30}$ sample with Co domination, a typical GMR signal change with H_z is obtained. A low resistance state is obtained when H_z reaches its maximum. In this case, the Co moment in the CoTb layer and the Co moment of the free layer are aligned parallel, resulting in a low resistance state. Next, as H_z decreases and then increases along the opposite direction, reaching the range where H_z exceeds the coercivity of the Co layer but is still below the coercivity of the CoTb layer, the magnetic moment of Co is antiparallel to the net magnetic moment of the CoTb layer. The magnetic moments of the two Co atoms are antiparallel, resulting in a high resistance state. Interestingly, negative GMR ratios were observed in the $Co_{54}Tb_{46}$ sample with Tb-domination, as presented in Figure 3b. A high resistance state in the GMR signal is obtained when H_z reaches its maximum. This occurs because the net magnetic moment of the CoTb layer is opposite to the direction of its Co magnetic moment, resulting in the GMR signal response to

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the external magnetic field being opposite to that of the Co-dominant sample. The GMR ratio for the Co-dominant sample is over 88% higher than the 1.6% observed for the Tb-dominant sample. Details discussions on the reproducibility and stability of Co-dominant and Tb-dominant CoTb reference layer samples have been included in Supporting Information S4.

Furthermore, we conducted current-induced magnetization switching tests on Co-dominant and Tb-dominant devices. In these measurements, both samples were initially saturated at a H_z of ± 10 kOe. Subsequently, a series of current pulses with a duration of 500 μs were applied to the device in an external magnetic field of H_x = ± 800 Oe. Between each adjacent pulse, a test current of 3 × 10^{10} A/m^2 was used to monitor the changes in the MR. Figure 3c shows the current-driven magnetization reversal curves for the two devices under different conditions, as labeled in Figure 3c. Under the same measurement conditions, such as with the CoTb layer magnetized along the +z direction and H_x = 800 Oe, the dominant contributions from Co and Tb exhibit opposite switching behaviors, which are consistent with the opposing MR signals driven by H_z. The straight arrow illustrates the change from a Co-dominant device to a Tb-dominant device. When the initial magnetization direction is reversed to the −z direction, the switching polarity for both devices reverses, as illustrated by the curve arrow. Furthermore, when the initial magnetization direction is fixed but the direction of H_x, the polarity of the magnetization switching curve is reversed. This occurs due to the different effective fields induced by SOT under opposite H_x.[46,47] As observed here, for the Tb-dominant device which is under the same measurement conditions, the polarity of their magnetization reversal curves is opposite to that of the Co-dominant devices.[45,48] Tuning the composition of CoTb alloy to alternate the dominance between Co and Tb offers an additional approach for manipulating the nonvolatile memristive states. More details have been provided in Supporting Information S8.

2.3. Synaptic Behavior in Two Terminal GMR Memristive Devices. The behavior of artificial synapses using Co-dominated GMR devices with a high GMR ratio was simulated. The normalized magnetoresistance signal represents changes in the synaptic weights. Under an external magnetic field of H_x = − 800 Oe, positive current pulses with a duration of 500 μs and amplitudes gradually increasing from 1.87 × 10^{11} to 2.08 × 10^{11} A/m^2 were applied to simulate the LTP process in synaptic weights, as shown in Figure 4a in the orange-shaded region.[37,49] Subsequently, negative pulses with amplitudes ranging from 1.6 × 10^{11} to 1.78 × 10^{11} A/m^2 were simulated in the LTD process, depicted in the blue-shaded region. This process, repeated seven times, produced highly linear, symmetric, and reproducible curves, demonstrating the excellent synaptic plasticity of artificial synapses based on GMR devices. The calculations of nonlinearity factors for potentiation and depression are presented in Supporting Information S5.

To better evaluate the synaptic performance of the proposed GMR device, we utilized it to simulate a DNN for handwritten digit recognition, as shown in Figure 4b. A three-layer neural network was simulated with 784, 300, and 10 neurons in the input, hidden, and output layers, respectively.[27,39] In each recognition process, the handwritten digit images are converted into 28 × 28 pixels, which are then transformed into 784 signals as inputs for the neural network. The 10

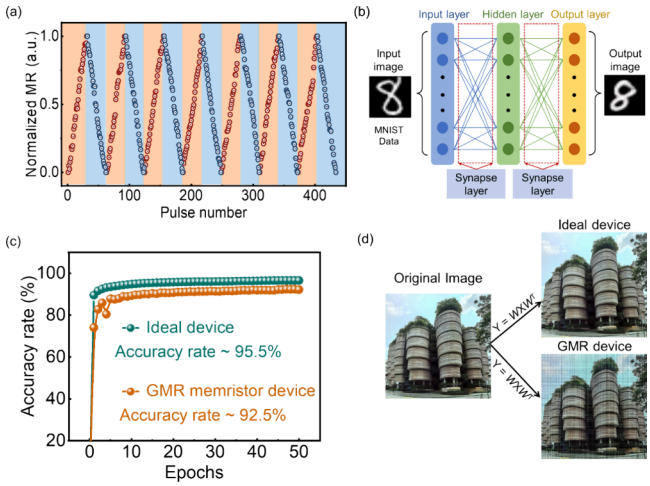

Figure 4. Simulation of the synaptic performance based on the GMR memristive device. (a) Normalized MR signal as changes in the artificial synaptic weight. (b) Schematic diagram of the DNN simulation structure. (c) Evolution of identification accuracy for the digital number based on the ideal device and resistance value in the proposed GMR device. (d) Visualization of programming error of proposed GMR device through the use of a 1024 × 1024 pixels RGB image and discrete Fourier transform.

neurons in the output layer correspond to the digits '0' to '9'. The neurons in the hidden layer use the "sigmoid" activation function, while the output layer employs the "softmax" activation function. Changes in the synaptic weight are implemented through the changes in the MR shown in Figure 4a. The accuracy rate of recognition based on the GMR device is 92.5%, slightly lower than that of the ideal device, 95.5%, as shown in Figure 4c. The accuracy of neural computing can be improved through the aspects: increasing the number of artificial synapses in the hidden layer; increasing the number of states in the linear change region of the artificial synapse; and improving the linearity of the linear region. For our GMR device, the weight change of the artificial synapse mainly depends on the domain wall motion of the free layer Co. However, the number of intermediate states of spintronic devices based on the domain wall motion mode is relatively small. At present, studies have shown that the magnetization switching mode of the Co layer can be transformed from domain wall motion to continuous nucleation mode by ion irradiation, which can effectively enhance the number of intermediate states and effectively enhance the linearity of the device.[35,39,50] Additionally, utilizing nucleated domain states enables further downscaling of the proposed GMR device from the micrometer to the nanometer scale.[39]

Next, the utilization of the discrete Fourier transform (DFT) to visualize the programming errors of the GMR device through DFT was performed, as illustrated in Figure 4d.[51] Initially, a 1024 × 1024 pixels RGB image was normalized to pixel brightness values between 0 and 255. Using the equation $Y = WXW^T$, where X represents the input image, Y is the output image, W represents the DFT transformation matrix, and W^T represents the transpose of matrix W, we applied DFT to the image twice. The first DFT transformed the image, and the second DFT served to reverse and reconstruct the image. Comparing the performance of the GMR device incorporating the programming errors to an ideal device without programming errors, we found that despite the errors, the

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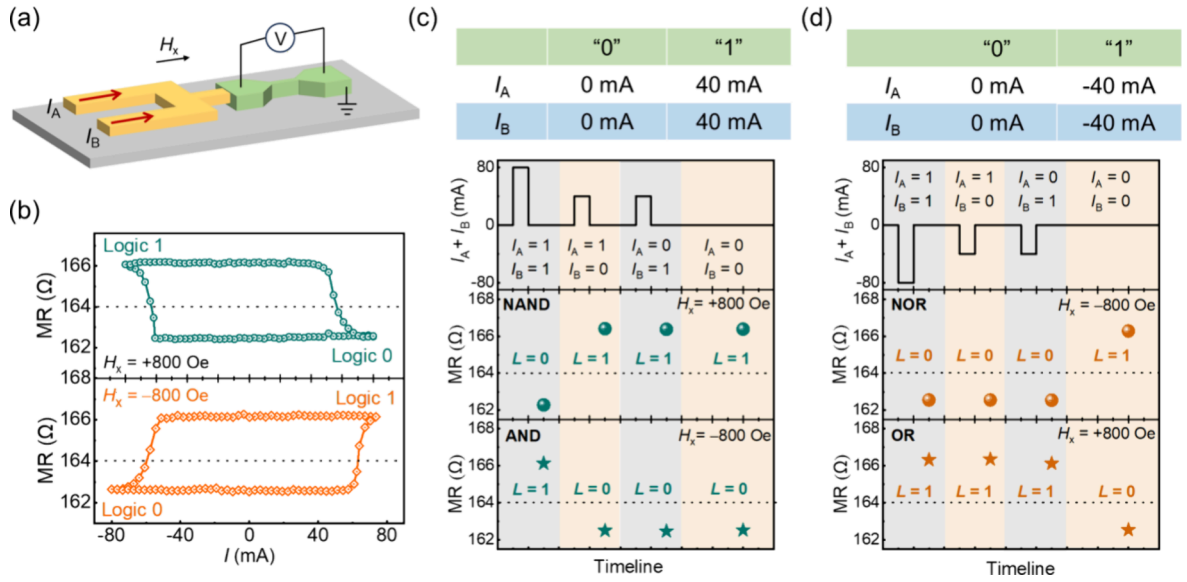

Figure 5. Demonstration of logic functionality based on the GMR memristive device. (a) Schematic of the logic using a single GMR device. (b) Current-induced different states in a Co-dominated GMR device. (c) Demonstration of NAND and AND logic gates with control of the input current. (d) Demonstration of NOR and OR logic gates with control of the input current.

GMR device still largely preserved the integrity of the original images.

2.4. Logic Function Based on the Two Terminal GMR Device. The basic logic gates using a single GMR device were implemented. As shown in Figure 5a, the logic device consists of a GMR device and two current inputs, labeled I_A and I_B. The value of MR was used as the logical output "L," with the high-resistance state defined as logic "1" and the low-resistance state defined as logic "0." Under an external magnetic field of +800 Oe, when $I_A + I_B = -80$ mA (-2.38×10^{11} A/m^2), the output switches to a high-resistance state; when $I_A + I_B = +80$ mA, it switches to a low-resistance state, as shown in Figure 5b. Under a magnetic field of $H_x = -800$ Oe, the situation is reversed. Figure 5c shows the logical representation of NAND and AND gates with an input of 0 mA defined as logic "0" and 40 mA as logic "1." A reset current pulse of $I_{reset} = -80$ mA was utilized to reset the state of the logic gates. Under a magnetic field of $H_x = +800$ Oe, when $I_A + I_B = 80$ mA, the output is in a low-resistance state (logic "0"). When $I_A + I_B$ is 40 or 0 mA, the output is in a high-resistance state (logic "1"), thus achieving the NAND logic. The implementation of the AND gate occurs under $H_x = -800$ Oe. For the NOR and OR gates, shown in Figure 5d, I_A and I_B are defined as logic "1" when both are − 40 mA, and as logic "0" when the current is 0 mA. The reset current is set at +80 mA. Under the $H_x = -800$ Oe, when both I_A and I_B are at 0 mA, the device outputs a high-resistance state (logic "1"); in other cases, the output is a low-resistance state (logic "0"), implementing the NOR gate logic. The OR gate is implemented under $H_x = +800$ Oe. Notably, in the magnetization switching curves shown in Figure 3, under the same initial magnetization state and external magnetic field conditions, changing the dominant element of the CoTb alloy can also alter the polarity reversal. A recent study has reported that growing CoTb alloy on PMN−PT substrates and applying voltage can effectively control ferrimagnetic CoTb alloy polarity.[52−55] Leveraging this feature, we propose a GMR logic device that uses the gate voltage and input current as parameters. This provides a new pathway for developing low-power, programmable spin logic devices.

CONCLUSIONS

We have demonstrated the innovative GMR memristive devices that harness SOT for information writing and GMR for information reading, enabling all storage, neuromorphic, and logic functions for advanced, scalable memristive memory. The GMR-based readout signal is enhanced by optimizing the Cu interlayer thickness. We successfully achieved ten distinct storage states in the Co-dominated GMR memristive device by varying driving current amplitudes and provided an approach to obtain more states with opposite polarity by tuning the composition of the CoTb layer. Furthermore, we demonstrated the functionalities of synaptic plasticity and Boolean logic, achieving high accuracy in handwritten digit recognition and image visualization tests based on this GMR device. Our findings exhibit the potential for realizing memristive memory with integrated logic functionality and highly scalable computing in a two-terminal GMR device.

METHODS

Sample Preparation. The GMR memristive stack of Ta (2 nm)/Pt (10 nm)/Co (1.6 nm)/Cu/$Co_{70}Tb_{30}$ (15 nm)/Ta (2 nm) and Ta (2 nm)/Pt (10 nm)/Co (1.6 nm)/Cu/$Co_{54}Tb_{46}$ (15 nm)/Ta (2 nm) were prepared on Si/SiO_2 substrate using ultrahigh vacuum AJA magnetron sputtering with base deposition pressures below 5×10^{-8} Torr. The Ta seed and capping layers were deposited using DC sputtering under 50 W power and 2 mTorr argon pressure at a deposition rate of 0.088 nm/s. The heavy metal Pt layer was deposited using DC sputtering under 50 W power and 2 mTorr argon pressure and at a deposition rate of 0.065 nnm/s. The CoTb reference layer was deposited using a cosputtering technique. For the deposition of $Co_{70}Tb_{30}$ and $Co_{54}Tb_{46}$ alloys, the sputtering power of the Co target was set at 50 and 25 W, respectively, with the sputtering power of the Tb target fixed at 50 W. The thickness of the Cu space layer was varied from 2 to 8 nm to optimize the GMR ratio, with the layer deposited at 50 W power and a rate of 0.075 nm/s. After film deposition, the planar two-terminal GMR devices were patterned by using maskless laser lithography.

MR, GMR Ratio, Exchange Field, Multistate Storage, and Synaptic Plasticity Measurements. For the MR measurement, a test current (I) with an amplitude of 1 mA was applied along the device. The delay time between the injection current and the

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measurement current is 1s. The lateral voltage signal (U) of the GMR device was measured using a 2182 voltmeter, and the magnetoresistance was calculated using the formula $R = U/I$. The MR vs. H_z change was measured by applying an in-plane direct current of 1 mA and recording the lateral resistance while sweeping the OOP field from −8 to +8 kOe. A Keithley 6221 provided the current sources, and a Keithley 2182 detected the lateral voltage, corresponding to resistance. This GMR ratio is defined as $\Delta R/R_{min}$, where ΔR represents the change in MR value from minimum to maximum, and R_{min} is the minimum value of MR. The exchange field between the free layer Co and the fixed layer CoTb was determined by aligning the magnetization direction of the CoTb layer along the $+z$ axis and conducting minor loop tests within the out-of-plane field range of ±1.5 kOe. The shift in the magnetic field indicates the magnitude of the exchange field. The same current source was used to apply current pulses for the multistate storage and synaptic plasticity measurements. There was a 1 ms delay between the application of the current pulse and the measurement of lateral MR.

Simulation of Handwritten Digit Recognition. The training data set consists of 60,000 labeled training examples and 10,000 labeled testing samples from MNIST. Each training image consists of 784 pixels, representing the input layer with 784 neurons. The 784 input signals (X_n) are expressed as pulse currents, thereby influencing the alteration of synaptic weights at the lateral MR resistance. Consequently, the value of the weights will pass to the hidden layer. The hidden layer had 300 neurons, and the output layer had 10 neurons. A sigmoid function, represented by $y = \frac{1}{1+e^{-x}}$, is selected as the activation function of the hidden layer. A softmax function, represented by $S(a) = \frac{e^{a_j}}{\sum_{k=1}^{N} e^{a_k}}$, where $\forall j \in 1 \cdots N$, and $N = 10$, is used as the activation function of the output layer. The accuracy rate is calculated by $\frac{N_R}{N_T}$, where the N_T is the total number of trained examples, and N_R will increase by one when the output neuron with the highest probability is the same as the label.

Visualization of Programming Errors. A 1024 × 1024 pixels RGB image was normalized to pixel brightness values between 0 and 255. Using the equation $Y = WXW^T$, where X represents the input image, Y represents the output image, W represents the DFT transformation matrix, and W^T represents the transpose of matrix W, we applied DFT to the image twice. The first DFT transformed the image, and the second DFT served to reverse and reconstruct the image. Comparing the performance of the GMR device incorporating the programming errors to that of an ideal device without programming errors, the performance was estimated despite the presence of the errors.

■ ASSOCIATED CONTENT

Data Availability Statement

The authors declare that all relevant data are included in the paper. Additional data are available from the corresponding authors upon reasonable request.

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.5c07283.

Comparison of readout signal with different spacer layers in the Co/spacer/$Co_{70}Tb_{30}$ GMR structure; demonstration of the enhanced GMR ratio; micromagnetic simulations on multiple magnetoresistance states; discussions on the reproducibility and stability of Co-dominant and Tb-dominant CoTb reference layers samples; nonlinearity factors calculation for potentiation and depression; neural network based on the proposed two-terminal GMR devices; effect of the reference layer CoTb composition on free layer Co domain wall (DW) motion and nucleation; current-induced switching with different initial magnetization states and external magnetic fields and comparison of the proposed architecture with existing state-of-the-art multiterminal memory architectures (PDF)

■ AUTHOR INFORMATION

Corresponding Authors

Tianli Jin − *School of Physical and Mathematical Sciences, Nanyang Technological University, Singapore 637371, Singapore; School of Integrated Circuits, Huazhong University of Science and Technology, Wuhan 430074, China;* orcid.org/0000-0002-9364-6024; Email: tianli.jin@ntu.edu.sg

Jiangwei Cao − *School of Physical Science and Technology, Lanzhou University, Lanzhou 730000, China;* Email: caojw@lzu.edu.cn

Wen Siang Lew − *School of Physical and Mathematical Sciences, Nanyang Technological University, Singapore 637371, Singapore;* orcid.org/0000-0002-5161-741X; Email: wensiang@ntu.edu.sg

Authors

Bo Zhang − *School of Physical and Mathematical Sciences, Nanyang Technological University, Singapore 637371, Singapore; School of Physical Science and Technology, Lanzhou University, Lanzhou 730000, China*

Dihua Wu − *School of Physics, Huazhong University of Science and Technology, Wuhan 430074, China*

Eng Kang Koh − *School of Physical and Mathematical Sciences, Nanyang Technological University, Singapore 637371, Singapore;* orcid.org/0000-0003-0733-7688

Funan Tan − *School of Physical and Mathematical Sciences, Nanyang Technological University, Singapore 637371, Singapore*

Calvin Xiu Xian Lee − *School of Physical and Mathematical Sciences, Nanyang Technological University, Singapore 637371, Singapore;* orcid.org/0000-0002-5426-2482

Ze Chen − *School of Physical and Mathematical Sciences, Nanyang Technological University, Singapore 637371, Singapore*

Gerard Joseph Lim − *School of Physical and Mathematical Sciences, Nanyang Technological University, Singapore 637371, Singapore;* orcid.org/0000-0003-2411-5841

Kaiming Cai − *School of Integrated Circuits and School of Physics, Huazhong University of Science and Technology, Wuhan 430074, China*

Complete contact information is available at: https://pubs.acs.org/10.1021/acsami.5c07283

Author Contributions

[⊥]T.J. and B.Z. contributed equally to this work.

Notes

The authors declare no competing financial interest.

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